REMARKS / AGRUMENTS

Applicant(s) respectfully traverse this rejection for the reasons set out below, and ask the Examiner for reconsideration.

Summary of the Office Action

Claims 1-2, 7, 12, 14-17, and 25-26 stand rejected under 35 U.S.C. 112 (first paragraph) as allegedly failing to comply with the enablement requirement.

Claim amendment

Dependent claim 26 that was previously denoted as claim 27 is now correctly denoted claim 26.

No new matter is introduced by this amendment.

Response to the 35 U.S.C. 112 rejection of claims 1-2, 7, 12, 14-17, and 25-26

Claims 1-2, 7, 12, 14-17, and 25-26 stand rejected under 35 U.S.C. 112 (first paragraph) as allegedly failing to comply with the enablement requirement.

The examiner argues that the specification does not disclose how the signal frequency and phase are maintained from the end of an ON period to the beginning of the following ON period in such a way as to an able one skilled in the art to which it pertains to make and/or use the invention.

Firstly, pertaining to claims 16, 17, and 26, the applicant maintains that these claims do not include the limitation referred to by the examiner, and thus should be allowed.

Pertaining to the other claims objected to by the examiner, the applicant respectfully maintains that the specification discloses to one who is skilled in the art in a utilizable way how the signal frequency and phase are maintained from the end of an ON period to the beginning of the following ON period.

Consider, for example, Figure 2, as well as the disclosure offered in the specification and cited below. Referring to the embodiment of the invention disclosed in relation to figure 2, one or more center frequencies are generated by one or more voltage-controlled oscillators (VCO, e.g. VCO 201). The center frequency is transmitted to multiple dividers (denoted 203 through 209) that are connected to the VCO, for outputting various multiples of the step frequency (of which the center frequency itself may be a multiple) via outputs of different dividers. It is noted that while dividers are normally used in a phase locked loop (PLL) to generate a single frequency, in the disclosed embodiment the dividers are used to generate multiple frequencies from a single center frequency (that are multiples of the step frequency).

As disclosed in paragraph 58, those multiple frequencies are inputted to a multiplexer (mux 212), which outputs to the a multiplier 213, wherein various multiples of the step frequency can be selected by the selection of different inputs to the multiplexer. The outputted signal is outputted via an output port denoted "out", from the multiplier which receives as a first input the output of the multiplexer, and as its second input the center frequency and outputs the selected step multiple multiplied by the center frequency.

As the frequencies and phases are determined prior to the multiplexing, to the mixing and to the transmitting, it is clear that only the at least VCO, as well as – according to an embodiment of the invention – at least some of the dividers, is required to be kept operating during OFF periods, while the power to other components (such as multiplexer 212, mixer 213 and the transmitting unit) can be switched or cycled off during OFF periods.

Citing paragraph 62, for example, it is disclosed that switching components off when not needed may improve (decrease) current consumption. For example, in some embodiments, during OFF periods of transmissions or receptions, power is switched or cycled off with respect to a transmitter, a receiver, or one or more components or circuits thereof.

The applicants maintain that one who is skilled in the art will straightforwardly recognize components of figure 2 (and generally of a transmitting unit as disclosed in the invention) – such as multiplexer 212, mixer 213, and potentially at least some of the dividers – that may be switched or cycled off during

OFF periods. Importantly, according to some embodiment of the invention, the phase is also dictated by the VCO (in response to the data signal, to the clock signal, or to a combination thereof), and thus all the components but the VCO may be switched or cycled off during OFF periods, when no fast switching is required, thus reducing the power consumption even more significantly.

It is noted that the solutions for transmitting information using ultra-wide band transmissions that are disclosed as parts of the invention enables the decreasing of power consumption by switching some of the components off during OFF periods, which are not enabled by other architectures and methods known in the prior art. The innovative architectures, methods, and systems that are disclosed in the invention facilitate such a decreased power reduction.

Therefore, claims 1-2, 7, 12, 14-17, and 25-26 should be allowed.

Conclusion

The applicant believes that in view of these arguments claims 1-2, 7, 12, 14-17, and 25-26 should be allowed, among which claims 16, 17, and 26, that do not include the limitation referred to by the examiner.

Respectfully submitted,

Date: June 18, 2008

/Oren Reches/

Oren Reches, Patent Agent #53506

Reches Patents,

Customer Number 69054